A. Introductory Comments

Based on the amendments and remarks to follow, reconsideration of this application is respectfully requested.

This amendment is in response to the first office action dated September 21, 2006. It is requested that Deposit Account No. 502158 be charged for any fee required for entry of this amendment.

When filed, this application contained 5 independent claims and 12 dependent claims. In response to a restriction requirement from USPTO, original claims 1-4 and 12-15 had been withdrawn from the patent application.

In this office action, claims 5-10 and 16-17 were rejected under 35 U.S.C. 102 (e) as being anticipated by Saluja et al. (US Patent No. 6,772,399). Further, claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Saluja et al. in view of CVC Lite User Manual.

In response to the rejections, claims 7-9 have been cancelled without prejudice or disclaimer. Claims 5, 6, 10, 11 and 16-17 have been amended and new claims 18 and 19 have been added as set forth in the next section.

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C. Remarks

Based on the above amendments and remarks to follow, reconsideration of this application is respectfully requested.

In this office action, claims 5-10 and 16-17 were rejected under 35 U.S.C. 102 (e) as being anticipated by patent to Saluja et al. (US Patent No. 6,772,399). Further, claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Saluja et al. in view of CVC Lite User Manual.

In response to the rejections, claims 7-9 have been cancelled without prejudice or disclaimer. Claims 5, 6, 10, 11 and 16-17 have been amended and new claims 18 and 19 have been added.

In order to more clearly define, and distinctly claim the present invention from the patent to Saluja et al., and to clarify the correspondence between the language of the claims and that of the specification, claims 5 and 10 have been amended. The claims as amended, recite that the method of the present invention relate to comparing two finite-precision arithmetic circuits for equivalence. A finite-precision arithmetic circuit is represented by a data flow graph and the two finite-precision arithmetic circuits are compared for equivalence by checking the equivalence of the corresponding data flow graphs. A finite-precision data flow graph is split into lossless sub-graphs of infinite-precision using the information loss at the edges of the data flow graph. Each of the lossless sub-graphs is assigned a level number in the topological order in the corresponding data flow graph. The two data flow graphs are checked for equivalence by comparing the lossless sub-graphs that are at the same level in the respective data flow graphs. The lossless sub-graphs at the same level are compared till the lossless sub-graphs at the last level are compared. The lossless sub-graphs are represented as expressions and the expressions are compared for equivalence using a theorem proving technique. The support for this recitation is found at pp-4, lines 14-15, pp-6, lines 4-11, pp-12, lines 5-9, pp-15, lines 11-18, pp-17, lines 10-13, and pp-19, lines 6-13 of the patent application.

In light of amendments to independent claim 5, claim 6 has also been amended

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to clarify the correspondence between the language of the claims and that of the specification. The support for this recitation is found at pp-14, lines 19-23 of the patent application.

Moreover, claims 7-9 have been cancelled without prejudice or disclaimer.

Further, claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Saluja et al. et al. in view of CVC Lite User Manual. In response to the rejections, claim 11 has been amended. According to amended claim 11, the CVC lite program is a theorem proving technique that is used to check the equivalence of expressions generated from lossless sub-graphs of infinite-precision arithmetic precision circuits. The expressions generated from lossless sub-graphs do not have finite edge widths. CVC lite program is used to the check the equivalence of expressions that do not have finite edge widths.

Further, independent claim 16 has been amended to recite a computer program product for comparing two finite-precision arithmetic circuits for equivalence, each finite-precision arithmetic circuit can be represented by a data flow graph and the two finite-precision arithmetic circuits are compared for equivalence by checking the equivalence of the corresponding data flow graphs. Claim 16 has been amended to particularly point out and distinctly claim the subject matter so as to eliminate the rejections under 35 U.S.C. 102(e). The support of these recitations is same as the support cited for the recitations in independent claim 5.

Moreover, claim 17 has been amended in light of amendments to claim 6. The support for this recitation can be provided by the support cited for the corresponding subject matter in claim 6.

Further, claim 18 is newly added as a dependent upon amended independent claim 5 to clearly explain the step of balancing of each of the lossless sub-graphs. The support for this recitation is found at pp-16, lines 5-22 and pp-17, lines 1-6 of the patent application.

Furthermore, claim 19 is newly added as a dependent upon amended independent claim 5 to clearly explain the step of leveling of each of the lossless sub-

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graphs. The support for this recitation is found at pp-17, lines 17-21 of the patent application.

The present invention

The method of the present invention relates to comparing two data flow graphs for checking equivalence of corresponding finite-precision arithmetic circuits without resorting to bit-level Boolean reasoning. Each of the two data flow graphs of finite-precision arithmetic circuits are split into lossless sub-graphs, the lossless sub-graphs representing infinite-precision arithmetic circuits. The data flow graphs are split into lossless sub-graphs using the information loss at the edges of the each of the two data flow graphs. In a data flow graph, the information loss at an edge is measured using the information content and required precision at that edge. The lossless sub-graphs that are formed after splitting are assigned a level number in the corresponding data flow graph. The level number is the order of existence of a lossless sub-graph in the corresponding lossless sub-graph. The level numbers are assigned to lossless sub-graphs in a topological order in the corresponding data flow graphs. Further, the lossless sub-graphs at the same level are compared for equivalence. If the lossless sub-graphs at a particular level are equal, then the lossless sub-graphs at the next higher level are compared for equivalence. The two data flow graphs are equal if the corresponding sub-graphs at the same level are equal. A theorem proving technique such as CVC lite program can be used for checking the equivalence of the lossless sub-graphs, as the lossless sub-graphs represent infinite-precision arithmetic circuits and do not have finite edge widths. The lossless sub-graphs can be converted into expressions, and the expressions can be compared using the CVC lite program. The support for this recitation is found at pp-4, lines 3, lines 12-19, pp-4, lines 14-15, pp-6, lines 4-11, pp-12, lines 5-9, pp-15, lines 11-18, pp-17, lines 10-13, and pp-19, lines 6-13 of the patent application.

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The prior art

In contrast, the patent to Saluja et al. (US Patent No. 6,772,399) includes a method and system for optimizing a single data flow graph by reducing edge widths and maximizing the number of datapath operations that can be merged. Further, the patent to Saluja et al. provides a method and system for optimizing a data flow graph (DFG), by selecting an output port in the DFG and identifying a directed path to the selected output port. Further, the width of the selected output port is used to determine a minimum width that is required for at least one portion of the directed path. Further, one or more mergeable clusters in the DFG are identified that correspond to the determined minimum width. Finally, the mergeable clusters are used for generating data, which is further used in designing a circuit. In the system presented by Saluja et al., each cluster represents a group of datapath operators, for example, a cluster can be represented by sum of addends. A method of partitioning a data flow graph into maximal mergeable clusters is defined which allows the transformed data flow graph to have potentially smaller widths (bitwidths) of datapath operators and potentially greater mergeability of datapath operators.

However, the patent to Saluja et al. does not disclose any method for comparing two data flow graphs for checking equivalence of two finite-precision arithmetic circuits without resorting to bit-level Boolean reasoning. The patent to Saluja et al. provides a method of partitioning a data flow graph into maximal mergeable clusters, wherein clusters represent group of datapath operators. However, the patent to Saluja et al. does not disclose any method for identifying edges with information loss and using them to split a data flow graph of finite-precision into lossless sub-graphs of infinite-precision. In addition, the patent to Saluja et al. does not disclose a method of leveling the lossless sub-graphs in a topological order in order to facilitate the comparison of lossless sub-graphs that are at the same level, across the data flow graphs that are being compared. Also, the patent to Saluja et al. does not disclose a method for checking the equivalence of two data flow graphs by comparing the leveled lossless

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sub-graphs.

Further, the patent to Saluja et al. in view of CVC lite user manual does not disclose checking the equality of the two finite-precision arithmetic circuits by using a CVC program. The CVC program is a theorem proving technique that can only check the equivalence of the expressions that do not have finite edge widths. The CVC program cannot check the equality of the two finite-precision arithmetic circuits, as the expressions generated from the finite-precision arithmetic circuits have finite edge widths. The present invention provides a method for checking the equivalence of the two finite-precision arithmetic circuits. A method is provided for splitting the data flow graphs of the two finite-precision arithmetic circuits into lossless sub-graphs of infinite-precision arithmetic circuits. Further, a method is provided for comparing the two data flow graphs by using the corresponding lossless sub-graphs. The CVC program is used by the invention for comparing the lossless sub-graphs of infinite-precision arithmetic circuits. However, the invention does not use the CVC program for comparing the data flow graphs of finite-precision arithmetic circuits.

Therefore, in view of the amendments to independent claims 5 and 16 and the addition of new claims 18 and 19, and in light of the above discussion, the present invention as described in the present claims is patentable over patent to Saluja et al. In light of the amendments to independent claims 5 and 16, dependent claims 6, 10 and 17 and newly added claims 18 and 19, should be allowable.
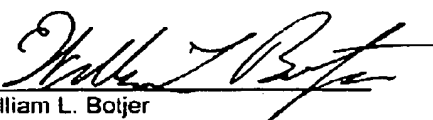
Therefore, it is evident that the method for optimizing a single data flow graph by reducing edge widths and maximizing the number of datapath operations that can be merged, in the patent to Saluja et al. is completely distinct from the present invention. Further, in light of amendments to claims 11, the present invention as described is patentable over Saluja et al. in view of CVC Lite User Manual.

The present claims have been amended to highlight the distinctions of the present invention over the prior art and it is respectfully submitted that the claims are now clearly patentable over the art of record, and notice to that effect is earnestly solicited, If the Examiner has any questions regarding this matter, the Examiner is requested to telephone applicants attorney at the numbers listed below prior to issuing

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a further action.

Dated: December 20, 2006   Respectfully Submitted,

By _____

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